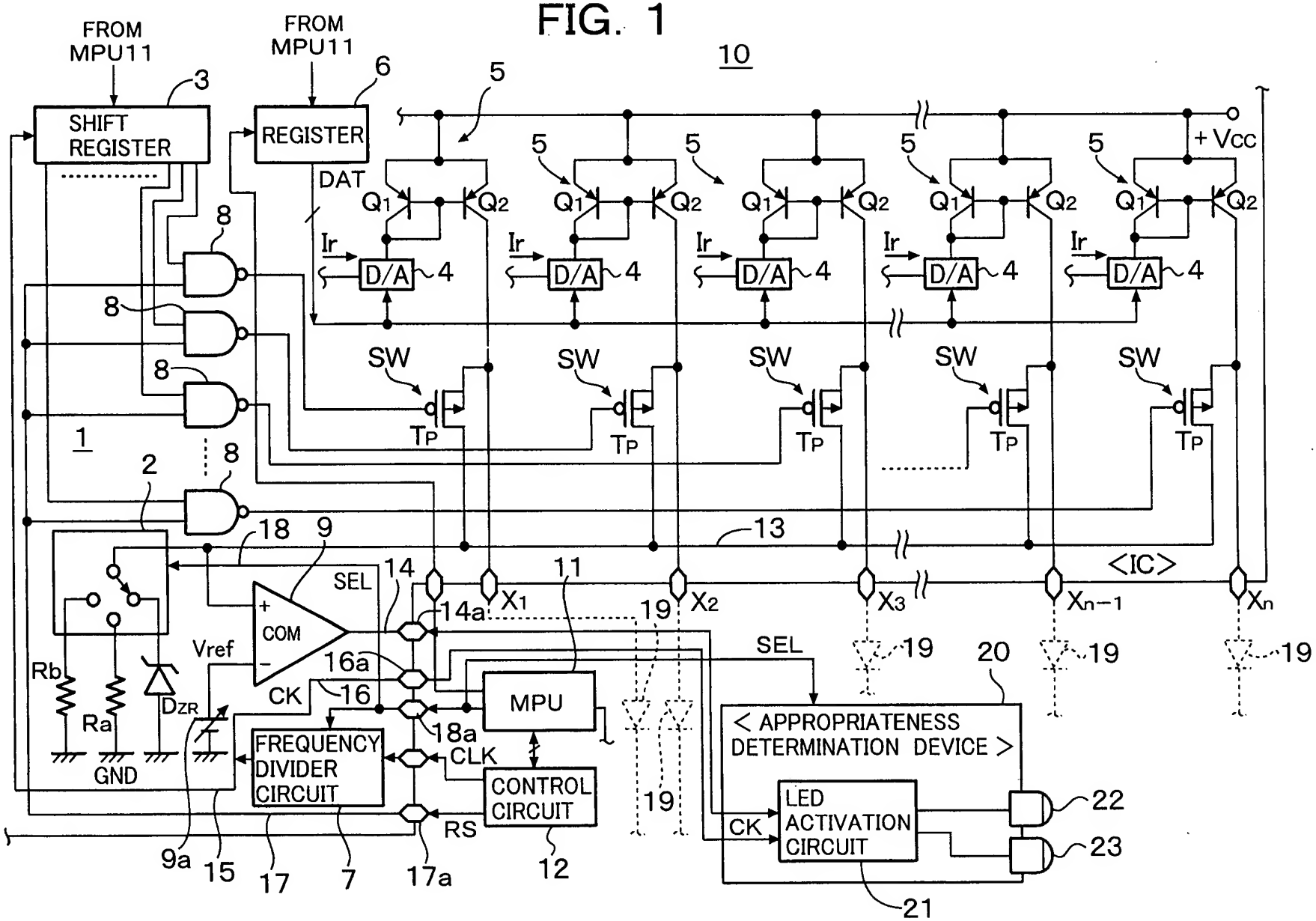
FIG. 1


FROM MPU11
FROM MPU11
10
SHIFT REGISTER
3
REGISTER
6
5
DAT
+ Vcc
Q1
Q2
Ir
D/A
4
8
SW
TP
1
2
18
9
13
<IC>
SEL
14
11
+
COM
−
Vref
14a
X1
X2
X3
Xn−1
Xn
19
16a
CK
16
MPU
18a
SEL
20
Rb
Ra
DZR
GND
FREQUENCY DIVIDER CIRCUIT
CLK
CONTROL CIRCUIT
RS
< APPROPRIATENESS DETERMINATION DEVICE >
LED ACTIVATION CIRCUIT
CK
22
23
21
9a
15
17
7
17a
12